App. Serial No. 10/796,480
Docket No.: US030080 US

In the Claims:

Please amend claim 1, 14, 23 and 29 as indicated below. This listing of claims replaces all prior versions.

1. (currently amended) For use in controlling routing circuitry having configurable test signal routing paths with controllable switches ~~(805, 808)~~ therein for coupling test signals between dedicated test-signal circuitry ~~(830)~~ and a target circuit device ~~(870)~~, a circuit configurator arrangement comprising:

a test-signal sense circuit ~~(831)~~ ~~adapted~~ to detect test signals carried by at least one of the test signal routing paths;

a switch-control interface circuit ~~(842)~~ ~~adapted~~ to control the controllable switches; and

a control logic circuit ~~(840)~~ ~~adapted~~ to send control signals to the switch-control interface circuit, in response to the detected test signals carried by said at least one of the test signal routing paths, and therein ~~adaptively~~ control routing of test signals in the configurable test signal routing paths.

2. (Original) The circuit configurator arrangement of claim 1, further comprising a communications link adapted to communicatively couple the control logic circuit to an external user-controlled device for passing reconfiguration-control signals to the control logic circuit, the control logic circuit being adapted to respond to the reconfiguration-control signals by sending control signals to the switch-control interface circuit for adaptively controlling the routing of the test signals in the configurable test signal routing paths.

3. (Original) The circuit configurator arrangement of claim 2, further comprising a memory adapted to store the reconfiguration-control signals for access by the control logic circuit, the stored reconfiguration-control signals, when executed, causing the control logic to send control signals to the switch-control interface circuit for adaptively controlling the routing of the test signals in the configurable test signal routing paths.

4. (Original) The circuit configurator arrangement of claim 2, wherein the communications link is further adapted for reporting characteristics of the configured test signal routing paths to the external user-controlled device.

5. (Original) The circuit configurator arrangement of claim 1, further comprising a memory adapted to store said control signals for access by the control logic circuit, the stored control signals, when executed, causing the control logic to send signals to the switch-control interface circuit for adaptively controlling the routing of the test signals in the configurable test signal routing paths.

6. (Original) The circuit configurator arrangement of claim 1, wherein the test-signal sense circuit is adapted to detect test signals passing between the configurable test signal routing paths and an external circuit and wherein the control logic circuit is adapted to adaptively control routing of test signal between the configurable test signal routing paths and the external circuit, in response to the detected test signals.

7. (Original) The circuit configurator arrangement of claim 1, wherein the dedicated test-signal circuitry includes a test-data input port adapted to receive test data, a test-data output port adapted to pass test data from the dedicated test-signal circuitry and a test-clock port.

8. (Original) The circuit configurator arrangement of claim 1, wherein the control logic circuit is programmed to control and monitor a plurality of operational characteristics of the configurable test signal routing paths.

9. (Original) The circuit configurator arrangement of claim 1, wherein the configurable test signal routing paths include a plurality of JTAG signal path switches adapted to route JTAG signals on the routing circuitry and between the routing circuitry and an external circuit, and wherein the control logic circuit is programmed to send the control signals to configure the plurality of JTAG signal path switches.

10. (Original) The circuit configurator arrangement of claim 9, wherein the control logic circuit is programmed to switch the plurality of JTAG signal path switches in response to reconfiguration-control signals received from an external user-controlled device.

11. (Original) The circuit configurator arrangement of claim 1, wherein the control logic circuit is adapted to monitor operational characteristics of the routing circuitry prior to power-up of the routing circuitry.

12. (Original) The circuit configurator arrangement of claim 1, wherein the control logic circuit is adapted to send control signals to the switch-control interface circuit and therein set the controllable switches, prior to power-up of the routing circuitry.

13. (Original) The circuit configurator arrangement of claim 1, wherein the control logic circuit is further adapted to control a JTAG controller for generating JTAG test signals and adaptively control the routing of the generated JTAG test signals in the configurable test signal routing paths.

14. (currently amended) For use with a configured circuit ~~(110)~~ having a plurality of controllable switches ~~(115)~~ communicatively coupled between at least two JTAG test nodes ~~(112, 114)~~ on JTAG signal paths and target circuit devices along the JTAG signal paths, a circuit configurator arrangement ~~(100)~~ comprising:

a communications port ~~(130)~~ ~~adapted~~ to accept control inputs from a user interface ~~(140)~~ via a communications link and to provide output data to the user via the communications link;

a test-signal sense circuit ~~(126)~~ ~~adapted~~ to detect JTAG test signals carried by at least one of the test signal routing paths;

a memory ~~(122)~~ having computer-executable code; and

a programmable microcontroller ~~(120)~~ communicatively coupled to the configured circuit, the communications port and the test signal sense circuit, wherein the computer-executable code, when executed, causes the microcontroller to control the controllable switches for coupling JTAG test signals to the target circuit devices in response to test

signals sensed by the test-signal sense circuit, and to monitor operational characteristics of the configured circuit and output data to the user interface ~~140~~ in response to the monitored operational characteristics.

15. (Original) The circuit configurator arrangement of claim 14, wherein the microcontroller is programmed to cause the test-signal sense circuit to monitor the JTAG test nodes using an interrupt routine for automatically detecting test signals at the JTAG test nodes.

16. (Original) The circuit configurator arrangement of claim 14, wherein the microcontroller is programmed to control the controllable switches for routing JTAG test data between the configured circuit and an external configured circuit, via the JTAG test nodes.

17. (Original) The circuit configurator arrangement of claim 14, wherein the microcontroller is adapted to control the controllable switches in response to control inputs received from the user interface via the communications port.

18. (Original) The circuit configurator arrangement of claim 14, wherein the circuit configurator arrangement is adapted to receive computer-executable code from the user interface via the communications port and to store the computer-executable code in the memory, the received and stored computer-executable code, when executed, causing the microcontroller to control the controllable switches.

19. (Original) The circuit configurator arrangement of claim 14, wherein the microcontroller is programmed to perform diagnostic testing on the configured circuit when the configured circuit is not powered and to report the results of the diagnostic testing via the communications port.

20. (Original) The circuit configurator arrangement of claim 19, wherein the microcontroller is programmed to report an error signal in response to the diagnostic testing indicating an error in the routing circuitry.

21. (Original) The circuit configurator arrangement of claim 19, wherein the microcontroller is adapted to perform diagnostic testing on timing circuits coupled to the routing circuitry by detecting clock frequency thereof and, in response to detecting an improper clock frequency, to report an error signal indicating a timing error.

22. (Original) The circuit configurator arrangement of claim 14, further comprising an analog-to-digital converter (ADC) coupled to the configured circuit and adapted for converting detected analog signals thereon to digital signals, the microcontroller being further adapted for reporting characteristics of the configured circuit in response to the digital signals.

23. (currently amended) For use in a prototype arrangement of inter-connectable circuit boards, each of the inter-connectable circuit boards having JTAG test signal routing switches ~~(115)~~, at least two JTAG circuit paths and JTAG input/output (I/O) test nodes ~~(112, 114, 116, 118)~~ for passing JTAG test signals to and from other inter-connectable circuit boards ~~(150, 160)~~, a configurator circuit comprising:

a memory ~~(122) adapted~~ to store data including computer-executable code;

a microcontroller ~~(120)~~ on a first one of the inter-connectable circuit boards and communicatively coupled to the memory, the computer-executable code, when executed, causing the microcontroller to:

monitor the JTAG I/O test nodes to detect connectivity to another inter-connectable circuit; and

automatically configure the JTAG test signal routing switches in response to the JTAG I/O test node monitoring for routing JTAG test signals along a JTAG circuit path on at least the first one of the inter-connectable circuit boards; and

a communications link ~~(130) adapted~~ to communicate control inputs from a user interface device ~~(140)~~ to the microcontroller and to communicate outputs from the microcontroller to the user interface, the microcontroller being operable in response to the control inputs.

24. (Original) The configurator circuit of claim 23, wherein the computer-executable code, when executed, causes the microcontroller to monitor the JTAG I/O test nodes and, in

response to detecting connectivity to another inter-connectable circuit via the monitoring, to set the controllable switches for routing JTAG test signals between the inter-connectable circuits.

25. (Original) The configurator circuit of claim 23, wherein the computer-executable code, when executed, causes the microcontroller to monitor the JTAG I/O test nodes and, in response to detecting that another inter-connectable circuit is not connected to a particular JTAG test node via the monitoring, to set the controllable switches for routing away from the particular JTAG test node.

26. (Original) The configurator circuit of claim 23, wherein the microcontroller is adapted to set the JTAG test signal routing switches in response to control inputs received from the user interface.

27. (Original) The configurator circuit of claim 23, wherein the computer-executable code, when executed, causes the microcontroller to perform an interrupt routine for monitoring the JTAG I/O test nodes.

28. (Original) The configurator circuit of claim 23, wherein the computer-executable code, when executed, causes the microcontroller to perform a data-polling routine for monitoring the JTAG I/O test nodes.

29. (currently amended) For use in controlling routing circuitry having configurable test signal routing paths with controllable switches ~~(805, 808)~~ therein for coupling test signals between dedicated test-signal circuitry ~~(830)~~ and a target circuit device ~~(870)~~, a circuit configurator arrangement comprising:

test-signal sensing means ~~(831)~~ for detecting test signals carried by at least one of the test signal routing paths;

switch-control interface means ~~(842)~~ for controlling the controllable switches; and control logic means ~~(840)~~ for sending control signals to the switch-control interface circuit, in response to the detected test signals carried by said at least one of the test signal routing

paths, and therein ~~adaptively~~ control routing of test signals in the configurable test signal routing path.